REMARKS

This is a full and timely response to the outstanding FINAL Office Action mailed February 3, 2009. The Examiner is thanked for the thorough examination of the present application. Upon entry of the amendments in this response, claims 1-6, 13, 16-24, 32, 33, and 35-38 are pending in the present application. Applicants respectfully request consideration of the following remarks contained herein. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

I. Summary of Telephone Interview with Examiner

Applicants wish to thank Examiner Do for the time spent with Applicants' representative (Jeffrey Hsu, Reg. No. 63,063) during a telephone interview conducted on March 12, 2009 regarding the above-identified Office Action. During the interview, the rejections under 35 U.S.C. §101 and 35 U.S.C. §103(a) were discussed. Various potential amendments were discussed to address the §101 rejection of claim 20. Potential amendments were also discussed with regards to the §103 rejection of the remaining claims. Applicants thank Examiner Do for indicating what he believes are the patentable features in claim 20. Based on this, a tentative agreement was reached with Examiner Do that the proposed amendments would be sufficient to overcome the cited rejections. Applicants submit that the amendments and remarks set forth herein are consistent with those raised during the interview.

II. Response to Claim Rejections Under 35 U.S.C. § 112

Claims 13, 16, 32-33, and 35 are rejected under 35 U.S.C. 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which application regards as the invention. In an effort to clarify the step of "assigning" recited in both claims 13 and 32, Applicants have amended these claims to now recite the step of "initializing." On page 2, the Office Action asserts that it is not clear how the step of assigning the destination register at the beginning relates to the other steps (comparing, concatenating, etc.) as whatever is stored in the destination register would be overwritten by the last step of storing. Applicants point out, however, that the concatenating and storing steps are performed conditionally, as clearly reflected in the claim language. Claim 13, for example, recites "concatenating the value stored in the source register with an index value associated with the source register and storing the concatenated value in the destination register *when the value stored in the source register is less than the value stored in the destination register*." The destination register is conditionally written to and stores a value that is compared to the value in the source register. The destination register is initially assigned an index value and a value of a first source register from among the plurality of source registers. In this regard, Applicants believe that there is a clear relationship between the initialization step and the remaining steps recited in claim 13. Based on the foregoing, Applicants respectfully request that the §112 rejections be withdrawn.

III. Response to Claim Rejections Under 35 U.S.C. § 101

Claims 1-6, 13, 16, 20-24, 32-33, and 35 are rejected under 35 U.S.C. 101 because the claimed invention is allegedly directed to non-statutory subject matter. Applicants thank the Examiner for his input on addressing the §101 rejection.

With respect to claims 1 and 20, the Examiner appeared to indicate during the interview that Applicants do not disclose whether the means are implemented in hardware or merely software. If the "means for" elements are directed to software code, the claimed "means for" elements do not fall within any statutory categories. Applicants submit that the "means for" elements are expressed in "means" plus function format and are intended to be construed as determined in accordance with 35 U.S.C. § 112, paragraph 6. Claims 1 and 20 are clearly recited in means-plus-function format. Pursuant to 35 U.S.C. § 112, paragraph 6, a claim element recited in means-plus-function format "shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof." 35 U.S.C. § 112, paragraph 6.

The present specification describes specific structures (*i.e.,* hardware) for executing specific functions. As a non-limiting example, Applicants refer the Examiner to the various components (*e.g.,* comparator 822) depicted in FIGS. 7-9 for executing the processes described in the flow diagrams of FIGS. 1-6. In this regard, the "means for" elements recited in claims 1 and 20 are not merely software, but instead correspond to the described hardware and its equivalents for executing such software. For at least the reason that this interpretation of claims 1 and 20 is inconsistent with §112, paragraph 6, the rejection under § 101 should be withdrawn.

Furthermore, the Board of Patent Appeals and Interferences ("BPAI") has spoken on the issue of whether claims directed to a system having "means for" elements is a computer program per se. See *Ex parte Frederic Bauchot, Daniel Mauduit, and Benoit Sirot* (BPAI 2006) (hereinafter "*Ex parte Bauchot*"). Although not binding precedent in the present case, the BPAI stated in *Ex parte Bauchot* that the functions in claim 6, which was a means plus function claim, "clearly cannot read on software only because the functions can only be performed in cooperation with the computer hardware." *Id.* at 8. In the present case, the claims do not strictly read on software because the specification also describes hardware. For at least this additional reason, Applicants request that the rejection of claims 1 and 20 under 35 U.S.C. §101 be withdrawn.

Regarding claims 13 and 32, the Office Action alleges that the recited methods are not tied to a specific machine or apparatus. A claimed process is patent-eligible under 35 U.S.C. § 101 if: (1) it is tied to a particular machine or apparatus, or (2) it transforms a particular article into a different state or thing. See, *In re Bilski*, F.3d, 88 U.S.P.Q.2d 1385 (2008). As amended herein, claims 13 and 32 are clearly tied to a particular machine. In particular, claim 13 now recites: "A method implemented as instructions for manipulating a processor for reducing a number of processor cycles for determining a minimum value and a corresponding index value of a plurality of source registers of the processor, the method comprising the steps of. . ." Claim 32 now recites: "A method implemented as instructions executed by a processor for reducing a number of processor cycles for determining a maximum value and a corresponding index value of a plurality of source registers of the processor, the method comprising the steps of . . ." As such, Applicants submit that the claimed subject matter is

statutory under 35 U.S.C. §101 and respectfully request that the §101 rejections be withdrawn.

IV. Response to Claim Rejections Under 35 U.S.C. § 102

It is axiomatic that "[a]nticipation requires the disclosure in a single prior art reference of each element of the claim under consideration." *W. L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983). Therefore, every claimed feature of the claimed invention must be represented in the applied reference to constitute a proper rejection under 35 U.S.C. § 102.

Claims 13 and 32-33 are rejected under 35 U.S.C. §102(e) as allegedly being anticipated by *Okumura et al.* (U.S. Pat. No. 5,726,923, hereinafter "*Okumura*"). For at least the reasons set forth below, Applicants traverse these rejections.

A. Independent Claim 13

Applicants respectfully submit that independent claim 13 patently defines over *Okumura* for at least the reason that *Okumura* fails to disclose, teach, or suggest the features emphasized below in claim 13.

Claim 13 recites:

> 13. A method implemented as instructions for manipulating a processor for reducing a number of processor cycles for determining a minimum value and a corresponding index value of a plurality of source registers of the processor, the method comprising the steps of:
>
> initializing a destination register with an index value and a value of a first source register from among the plurality of source registers;
>
> for each of the plurality of source registers, comparing a value stored in the source register with a value stored in a destination register;

> concatenating the value stored in the source register with an index value associated with the source register and storing the concatenated value in the destination register when the value stored in the source register is less than the value stored in the destination register; and
>
> ***setting active status bits in the source register and in the destination register such that a value of a register having an active status is less than a value of a register having an inactive status***, wherein comparing, concatenating, and storing are implemented by a single processor instruction and performed within a single processor cycle by the processor.

(Emphasis added). During the telephonic interview, the Examiner indicated that claim 20 would be allowable, provided that the §101 rejection is addressed. The Examiner indicated that the features in claim 20 directed to the use of status bits were patentable. In an effort to advance prosecution, Applicants have thus amended claim 13 to recite the step of "setting active status bits in the source register and in the destination register such that a value of a register having an active status is less than a value of a register having an inactive status" and submits that *Okumura* fails to disclose, teach, or suggest this feature. Applicants note that in addressing dependent claim 6 on page 7, the Office Action alleges that the presence (or absence) of the index field in *Okumura* serves as a status bit. Even assuming, for the sake of argument, that this is equivalent to a status bit, *Okumura* fails to further disclose or suggest the limitation "a value of a register having an active status is less than a value of a register having an inactive status." Accordingly, Applicants respectfully submit that independent claim 13 patently defines over *Okumura*.

B. Independent Claim 32

Applicants respectfully submit that independent claim 32 patently defines over *Okumura* for at least the reason that *Okumura* fails to disclose, teach, or suggest the features emphasized below in claim 32.

Claim 32 recites:

> 32. A method implemented as instructions executed by a processor for reducing a number of processor cycles for determining a maximum value and a corresponding index value of a plurality of source registers of the processor, the method comprising the steps of:
> initializing a destination register with an index value and a value of a first source register from among the plurality of source registers;
> for each of the plurality of source registers,
> comparing a value stored in the source register with a value stored in a destination register;
> concatenating the value stored in the source register with an index value associated with the source register and storing the concatenated value in the destination register when the value stored in the source register is greater than the value stored in the destination register; and
> ***setting active status bits in the source register and in the destination register such that a value of a register having an active status is greater than a value of a register having an inactive status***, wherein comparing, concatenating, and storing are performed within a single processor cycle.

(Emphasis added). Applicants have amended claim 32 to incorporate features similar to those incorporated into claim 13 (and that are present in claim 20). As set forth above, the Examiner indicated during the telephonic interview that the subject matter in claim 20 relating to the use of status bits were patentable. In an effort to advance prosecution, Applicants have amended claim 32 to recite the step of "setting active status bits in the source register and in the destination register such that a value of a register having an active status is greater than a value of a register having an inactive

status" and submits that *Okumura* fails to disclose, teach, or suggest this feature. *Okumura* fails to disclose or suggest the limitation "a value of a register having an active status is greater than a value of a register having an inactive status." Accordingly, Applicants respectfully submit that independent claim 32 patently defines over *Okumura*. Furthermore, Applicants submit that dependent claim 33 is allowable for at least the reason that this claim depends from an allowable independent claim. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

V. Response to Claim Rejections Under 35 U.S.C. § 103

The USPTO has the burden under section 103 to establish a *prima facie* case of obviousness according to the factual inquiries expressed in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966). The four factual inquires, also expressed in MPEP §2141, are as follows:

(A) Determining the scope and contents of the prior art;

(B) Ascertaining the differences between the prior art and the claims in issue;

(C) Resolving the level of ordinary skill in the pertinent art; and

(D) Evaluating evidence of secondary considerations.

For a proper rejection of the claim under 35 U.S.C. §103, the cited combination of references must disclose, teach, or suggest all elements / features of the claim at issue. See, e.g., *In re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988) and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981). Claims 1-6 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Okumura*. Claims 16-19 and 35-38 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over

Okumura in view of the admitted prior art. For at least the reasons set forth below, Applicants traverse the rejections set forth.

C. Independent Claim 1

Applicants respectfully submit that independent claim 1 patently defines over *Okumura* for at least the reason that the combination fails to disclose, teach, or suggest the features emphasized below in claim 1.

Claim 1 recites:

> 1. A processor for reducing the processing effort for determining a minimum value of a plurality of values stored in source registers and determining an index value of a source register having the minimum value, the processor comprising:
> a destination register;
> a first source register storing a first value, wherein the first source register comprises S bits, and wherein the first value comprises N lower bits of the first source register;
> a second source register storing a second value, wherein the second source register comprises S bits, and wherein the second value comprises N lower bits of the second source register;
> means for comparing the first value stored in the first source register with the second value stored in the second source register;
> means for storing the first value in the destination register when the first value is less than or equal to the second value; and
> means for concatenating the index value with the second value into a concatenated value and storing the concatenated value in the destination register when the second value is less than the first value, wherein the index value is stored in an upper (S-N) bits of the concatenated value and the second value stored in the N lower bits of the concatenated value, ***wherein the first source register and the second source register each include an active status bit to indicate a status of the respective register, and wherein a value of a register having an active status is less than a value of a register having an inactive status***.

(Emphasis added). Applicants have amended claim 1 and canceled claim 6. No new matter is added. In addressing dependent claim 6 on page 7, the Office Action alleges that the presence (or absence) of the index field in *Okumura* serves as a status bit.

Even assuming, for the sake of argument, that these features are equivalent, *Okumura* fails to further disclose or suggest the limitation "a value of a register having an active status is less than a value of a register having an inactive status." Accordingly, Applicants respectfully submit that independent claim 1 patently defines over *Okumura*. Furthermore, Applicants submit that dependent claims 2-5 are allowable for at least the reason that these claims depend from an allowable independent claim.

D. Independent Claim 17

Applicants respectfully submit that independent claim 17 patently defines over *Okumura* in view of *Admitted Prior Art* for at least the reason that the combination fails to disclose, teach, or suggest the features emphasized below in claim 17.

Claim 17 recites:

> 17. A customer premise equipment (CPE) comprising:
> a network interface operably connected to a first network segment;
> a second network interface operably connected to a second network segment; and
> a processor operably connected to the network interfaces and being adapted to:
> compare a first value stored in ***a first source register*** of the processor with a second value stored in ***a second source register*** of the processor;
> store the first value in ***a first destination register*** of the processor when the first value is less than or equal to the second value; and
> store the second value in the first destination register of the processor and an index value in ***a second destination register*** of the processor when the second value is less than the first value, the index value representing the second source register.

(Emphasis added). In maintaining the rejection of claim 17, the Examiner states the following:

> *"Re claim 17, Okumura et al. disclose in Figures 1-9 a customer premise equipment (e.g. Figure 1 as general architecture) comprising: and a processor operably connected to the interfaces and being adapted to (e.g. for getting data into memory 1 in Figure 1): compare (e.g. by arithmetic logic unit 4 in Figure 1) a first value stored in* ***a first source register*** *of the processor (e.g. specific register 11 in Figure 1) with a second value stored in* ***a second source register*** *of the processor (e.g. registers 5-6 in Figure 1); store the first value in* ***a first destination register*** *of the processor when the first value is less than or equal to the second value (e.g. path when the specific register 11 is less than register 5 in Figure 3); and store the second value in the first destination register of the processor (e.g. value in register 6 in Figure 1) and an index value in* ***a second destination register*** *of the processor (e.g. corresponding index value of register 6 in Figure 1) when the second value is less than the first value (e.g. step S9 in Figure 3), the index value representing the second source register (e.g. Figure 2)."*

(Emphasis added; Office Action, page 8-9). As set forth above, the Office Action makes the following correlations:

"first source register" → "specific register 11" in *Okumura*
"second source register" → registers 5-6 in *Okumura*

It is not clear from the rejection, however, what components in *Okumura* correspond with the first and second destination registers. At most, either the first or second destination register corresponds with specific register 11 in *Okumura*. (See step S9 in FIG. 3.) However, the Office Action fails to account for both destination registers. In fact, the rejection does not appear to be complete, and does not read on claim 17 as a whole, taking into account all elements recited therein. Claim 17 explicitly recites two source registers and two destination registers in addition to a relationship between them (based on the values stored in the source registers, storing certain data in the destination registers). *Okumura* does not appear to disclose this. For example, claim 17 recites storing "the second value in the first destination register of the processor and

an index value in a second destination register." *Okumura*, however, fails to disclose this as *Okumura* fails to disclose storing the second value in one destination register and an index value in a second destination register. Step (S9) in FIG. 3 of *Okumura* clearly shows the both values being written to the **same** destination register (specific register 11) rather than to two destination registers. Furthermore, this deficiency is not addressed by the secondary reference (Applicants' admitted prior art.)

Accordingly, Applicants respectfully submit that independent claim 17 patently defines over *Okumura* in view of *Admitted Prior Art* for at least the reason that *Okumura* in view of *Admitted Prior Art* fail to disclose, teach or suggest the highlighted features in claim 17 above. Furthermore, Applicants submit that dependent claims 18-19 are allowable for at least the reason that these claims depend from an allowable independent claim.

E. Independent Claim 36

Applicants respectfully submit that independent claim 36 patently defines over *Okumura* in view of *Admitted Prior Art* for at least the reason that the combination fails to disclose, teach, or suggest the features emphasized below in claim 36.

Claim 36 recites:

> 36. A customer premise equipment (CPE) comprising:
> a network interface operably connected to a first network segment;
> a network interface operably connected to a second network segment; and
> a processor operably connected to the network interfaces and being adapted to:
> compare a first value stored in ***a first source register*** of the processor with a second value stored in ***a second source register*** of the processor;

> store the first value in ***a first destination register*** of the processor when the first value is greater than or equal to the second value; and
>
> store the second value in the first destination register of the processor and an index value in ***a second destination register*** of the processor when the second value is greater than the first value, the index value representing the second source register.

(Emphasis added). Applicants submit that arguments similar to those presented above for claim 17 apply to claim 36. (On page 10, the Office Action applies the same rationale in rejecting claim 36 as that used in rejecting claim 17). First, claim 17 explicitly recites a first source register, a second source register, a first destination register, and a second destination register. Further claim 17 recites storing "the second value in the first destination register of the processor and an index value in a second destination register of the processor when the second value is greater than the first value." However, step (S9) in FIG. 3 of *Okumura* clearly shows the both values being written to the **same** destination register (specific register 11) rather than to two destination registers. Furthermore, this deficiency is not addressed by the secondary reference (Applicants' admitted prior art.)

For at least this reason, Applicants respectfully submit that independent claim 36 patently defines over *Okumura* in view of *Admitted Prior Art* for at least the reason that *Okumura* in view of *Admitted Prior Art* fail to disclose, teach, or suggest the highlighted features in claim 36 above. Furthermore, Applicants submit that dependent claims 37 and 38 are allowable for at least the reason that these claims depend from an allowable independent claim.

F. Dependent Claims 16 and 35

Claims 16 and 35 stand rejected under 35 U.S.C. 103(a) as being unpatentable over *Okumura* in view of Applicants' *Admitted Prior Art*. As set forth above, Applicants submit that independent claims 13 and 32, from which claims 16 and 35 depend, respectively, are patentable over *Okumura*. Furthermore, Applicants' *Admitted Prior Art* fails to address the deficiencies expressed above for *Okumura*. As such, Applicants submit that independent claims 13 and 32 are patentable over the combination of *Okumura* in view of Applicants' *Admitted Prior Art*. Accordingly, dependent claims 16 and 35 are allowable for at least the reason that these claims depend from allowable independent claims.

CONCLUSION

Applicants respectfully submit that all pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephone conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 50-0835.

Respectfully submitted,

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